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Paper - CC12

Unit - 5

Topic - Synchronous counter with Parallel carry

(B) 4-Bit Synchronous Counter with Parallel Carry:

In it, toggle input (T=1) to each flip flop comes from an AND gate that has been excited

by the outputs from every preceding flip flop. In fig (4) a 4-bit Synchronous Counter with parallel carry is shown. We observe that each AND gate to FF/D will require three inputs Q_A, Q_B and Q_C. Similarly each AND gate to FF/C will require two inputs Q_A and Q_B. We note that:

(i) FF/A will toggle with each clock pulse. This is achieved by connecting J_A and K_A to a high level ($J_A = K_A = 1$, i.e., $J_A = 1$).

(ii) FF/B must change state whenever $Q_A = 1$. This is achieved by connecting J_B and K_B to Q_A.

(iii) FF/C changes state only when $Q_A = Q_B = 1$. For achieving it Q_A and Q_B are connected through AND gate to J_C and K_C, as shown in fig 4.

(iv) FF/D changes state only when $Q_A = Q_B = Q_C = 1$. This is achieved by connecting Q_A, Q_B and Q_C through AND gate to J_D and K_D.

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Table shown in fig 3(c) shows all the 16 states of the counter.